PCcardsDirect.com

SecureDigital™ Industrial Card

Product Specification

V3.0

Table of Contents:

1 Description

Our PCcardsDirect SecureDigital™ card supports the SD standard. This form factor is the perfect solution for data storage. It consists of a memory core and high performance controller, with wear-leveling technology and advanced file management to increase the transfer rate and life cycle of the memory core. It also provides Error Correcting Code (ECC) function to detect and correct errors automatically. Available in extended temperature rating.

1.1 Features

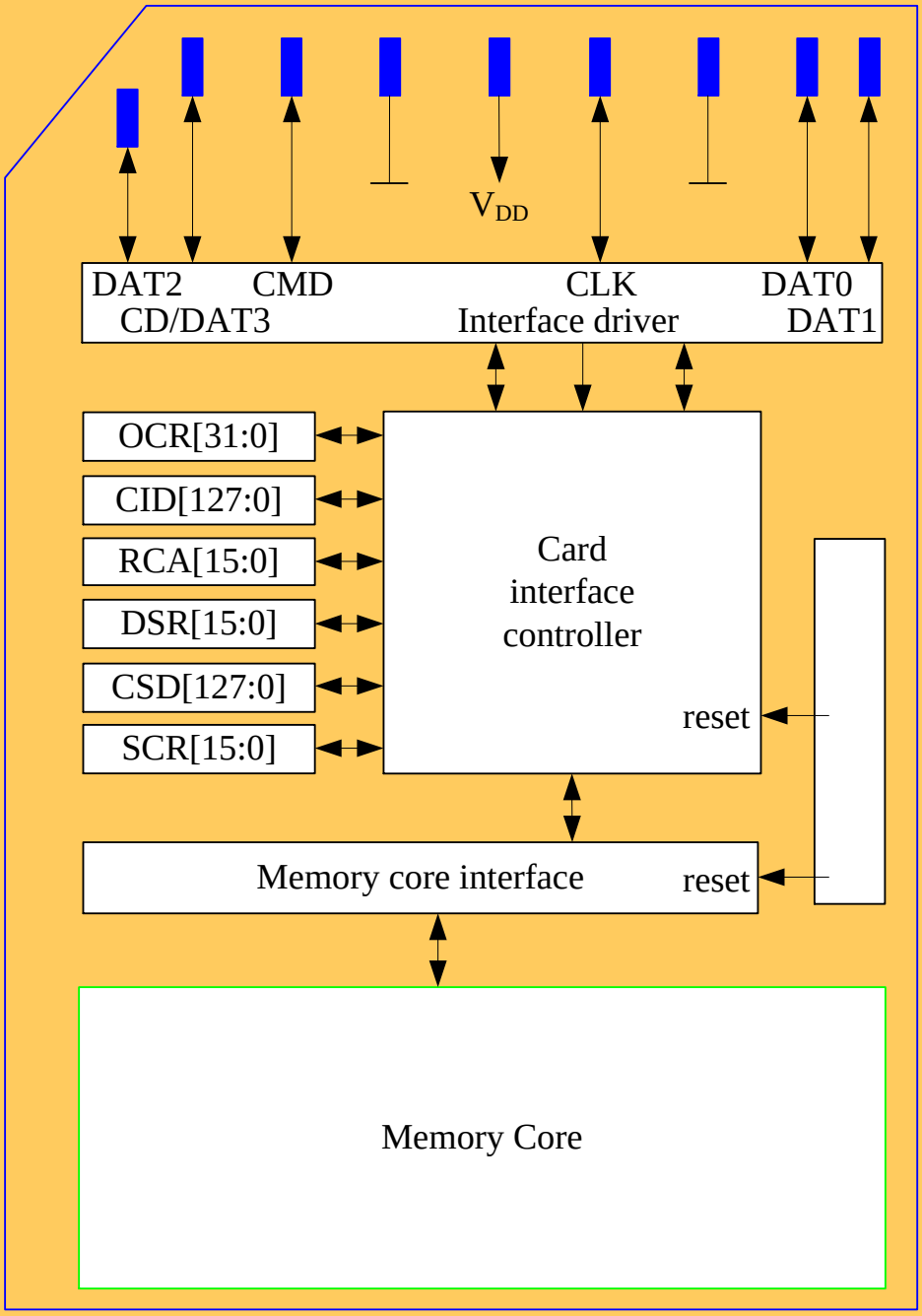
- Support the SD Standard Interface.
- Capacity： 512MB, 1GB, 2GB, 4GB, 8GB.
- Compatible with all PC Card Services and Socket Services.
- Support Error Correcting Code function to detect and correct errors.
- Support In System Programming (ISP) function to load the firmware.
- Support Wear Leverage function to maximize data endurance.
- Automatic error correction and retry capabilities.
- Supports power down commands and sleep modes.
- Very low power consumption.

1.2 System Specifications

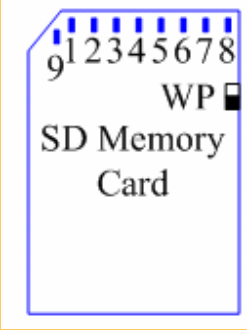
Interface		SD mode (1/ 4 bit), SPI
Number of Pins		9
Physical		
Length		32 ± 0.1mm
Width		24 ± 0.1mm
Thickness		2.1 ± 0.1mm
Weight		2.0 g
Power Requirement		
Voltage		2.7 V~3.6 V
Standby		500 μA (typ.)
Read		80 mA (typ.)
Write		80 mA (typ.)
Environment Specification		
Temperature	Operating	-25℃ ~ 85℃
	Storage	-65℃ ~ 100℃
Humidity	Operating	8% to 95%
	Storage	8% to 93%
Vibration	Operating	15 G peak-to-peak max
	Storage	15 G peak-to-peak max
Shock		1000 G max
Material		
PCB		FR4
SD lid		ABS
Switch		POM

2 Pin Assignments

2.1 Block Diagram



2.2 Pin Assignments



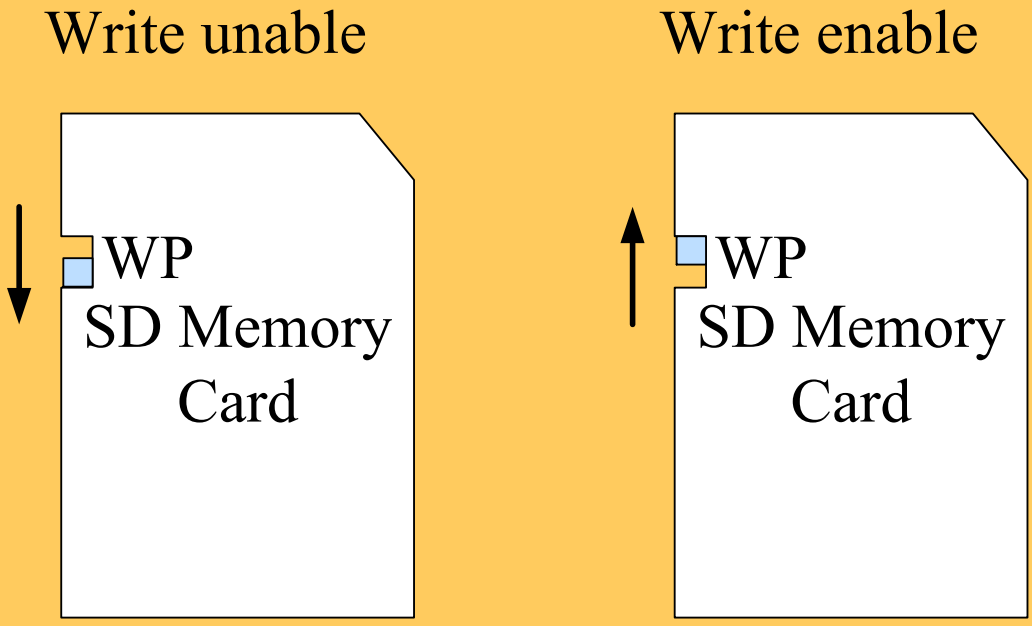
Pin	SecureDigital Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I	Chip Select (neg true)
2	CMD	PP	Command Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	V_{SS1}	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	V_{SS2}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit 2]	RSV		

1) S: power supply; I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high)

2) The extended DAT lines (DAT1-DAT3) are input on power on. They start to operate as DAT lines after SET_BUS-WIDTH command. The Host shall keep its own DAT1 -DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

3) After power up this line is input with 50K Ohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

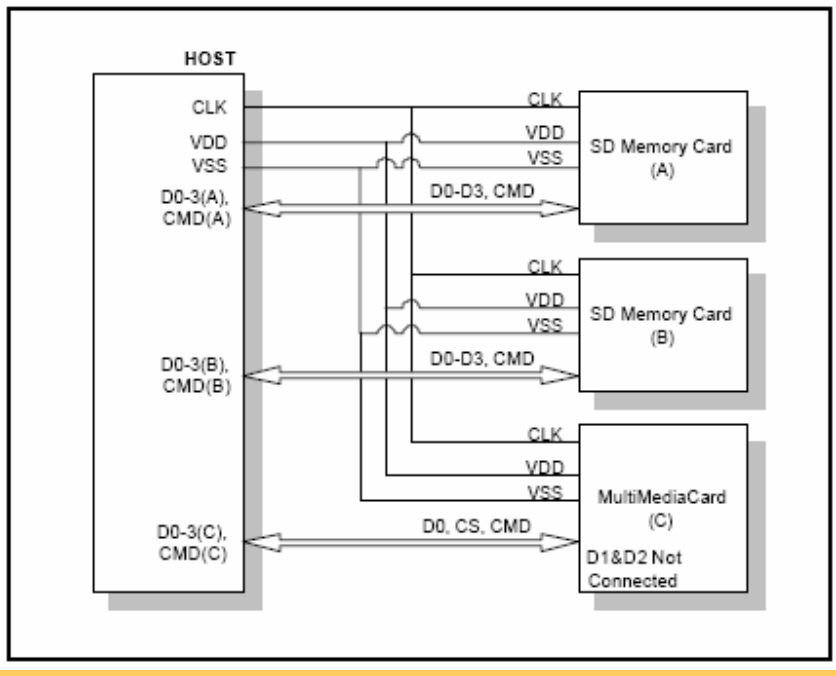
3 Card Function



4 Bus Topology

The SD Memory Card system defines two alternative communication protocols: SD and SPI. Applications can choose either one of modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, applications that use only one communication mode does not have to be aware of the other.

4.1 SD Bus



SD Memory Card System Bus Topology

The SD bus includes the following signals:

CLK: Host to card clock signal

CMD: Bi-directional Command/Response signal

DAT0 - DAT3: 4 Bi-directional data signals.

VDD, VSS1, VSS2: Power and ground signals.

The SD Memory Card bus has a single master (application), multiple slaves (cards), and synchronous star topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 - DAT3) signals are dedicated to each card providing continues point-to-point connection to all the cards.

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between HW cost and system performance.

4.2 SPI Bus

The SPI compatible communication mode of the SD Memory Card is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD mode which enables the wide bus option. The SD Memory Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the SD Memory Card SPI channel consists of the following four signals:

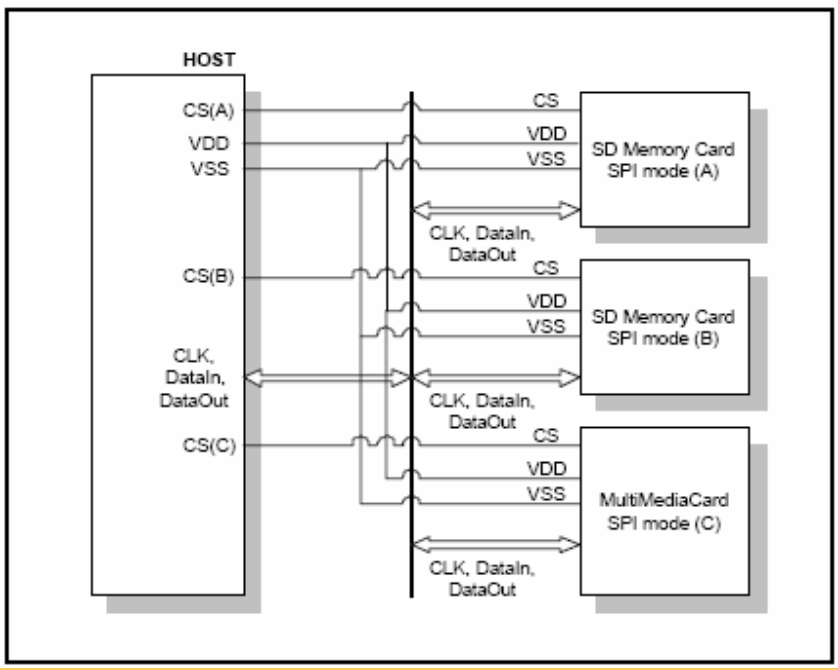
CS : Host to card Chip Select signal.

CLK : Host to card clock signal

Data In : Host to card data signal.

Data Out : Card to host data signal.

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.



SD Memory Card System SPI Mode Bus Topology

The card identification and addressing methods are replaced by a Chip Select (CS) signal. There are no broadcast commands. For each command, a card (slave) is selected by asserting (active low) the CS signal.

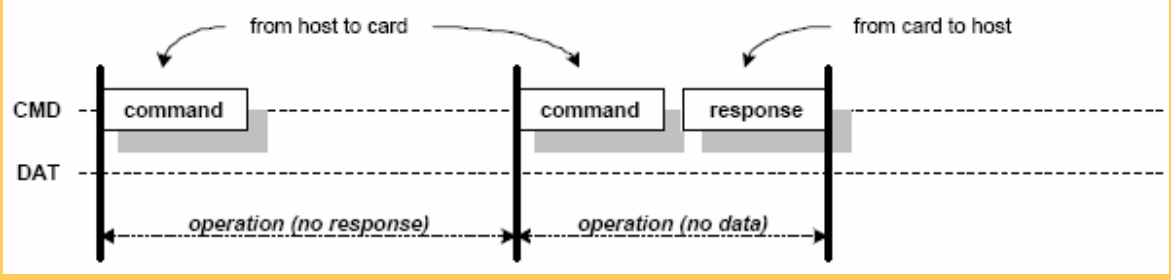
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can desert the CS signal without affecting the programming process.

The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

4.3 SD Bus Protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

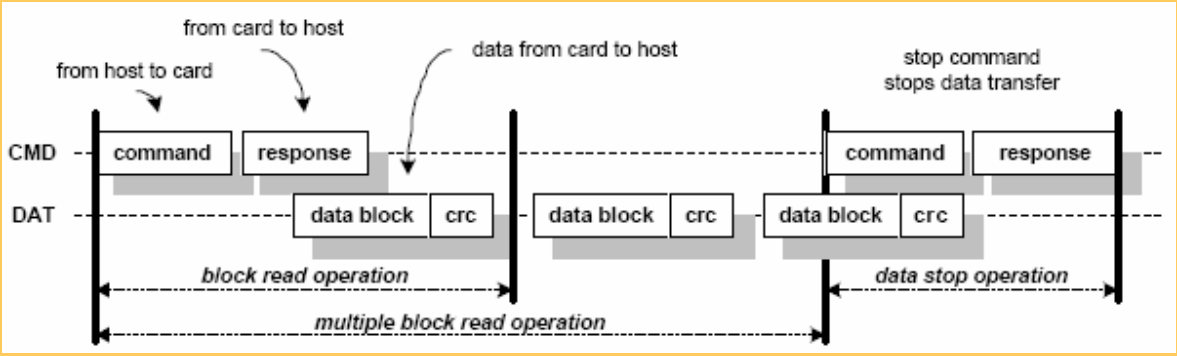


"no response " and "no data" Operations

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction. This type of bus transactions transfers their information directly within the command or response structure. In addition, some operations have a data token.

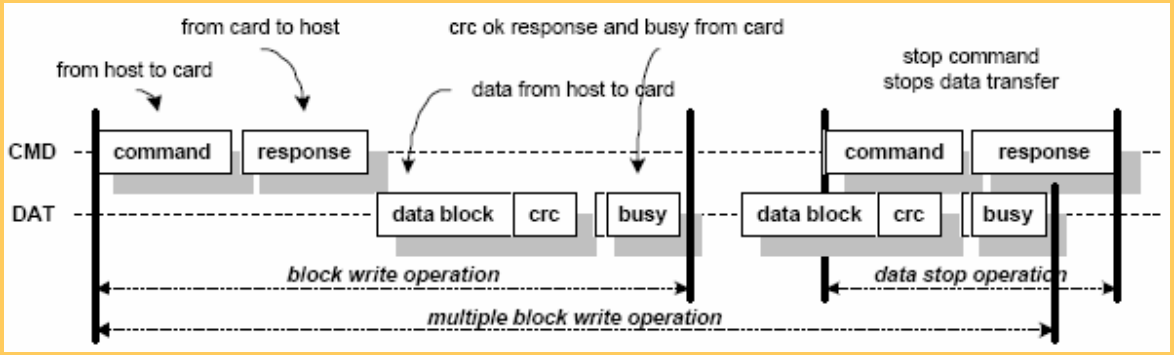
Data transfers to/from the SD Memory Card are done in blocks. Data blocks always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer

can be configured by the host to use single or multiple data lines (as long as the card supports this feature).



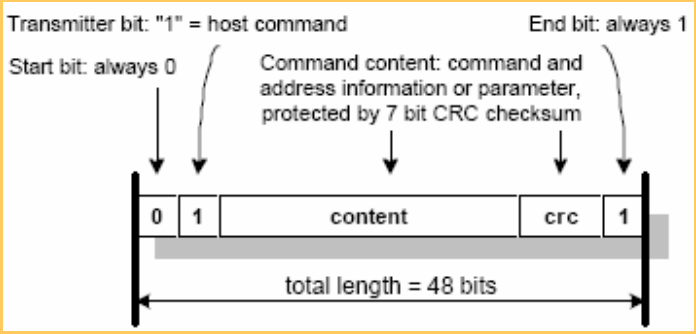
(Multiple) Block read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line regardless of the number of data lines used for transferring the data.



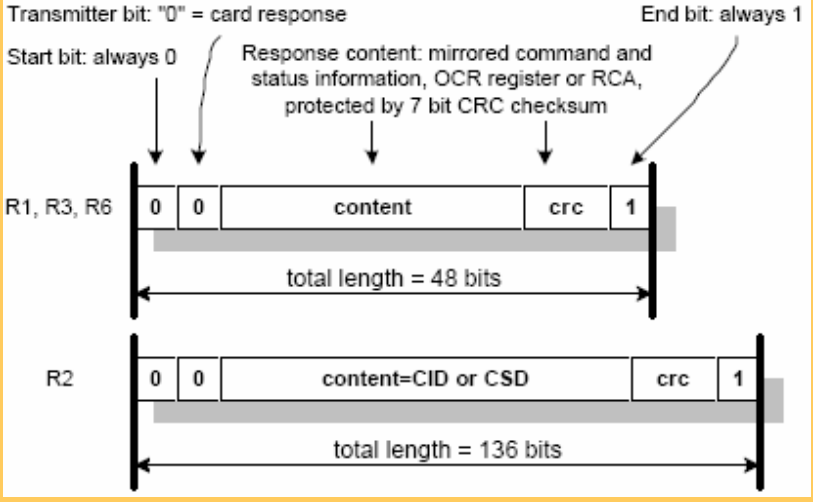
(Multiple) Block Write Operation

Command tokens have the following coding scheme:



Command Token Format

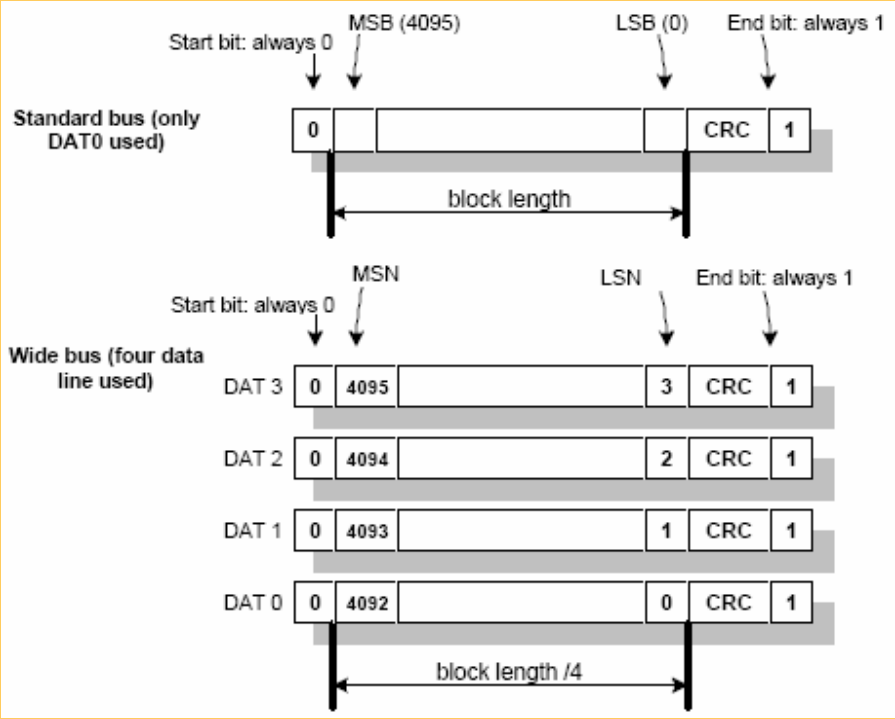
Each command token is preceded by a start bit (‘0’) and succeeded by an end bit (‘1’). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated. Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.



Response Token Format

In the CMD line, the MSB bit is transmitted first and the LSB bit is the last. When the wide bus option is used, the data is transferred 4 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for each one of the DAT lines. CRC bits are calculated and checked for each DAT line individually.

The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 are don't care during that period).



Data Packet Format

4.4 SPI Bus Protocol

While the SD channel is based on command and data bit streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Each command or data block is composed of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles).

Similar to the SD protocol, the SPI messages consist of command, response and data-block tokens. All communications between host and cards are controlled by the host (master). The host starts each bus transaction by asserting the CS signal low.

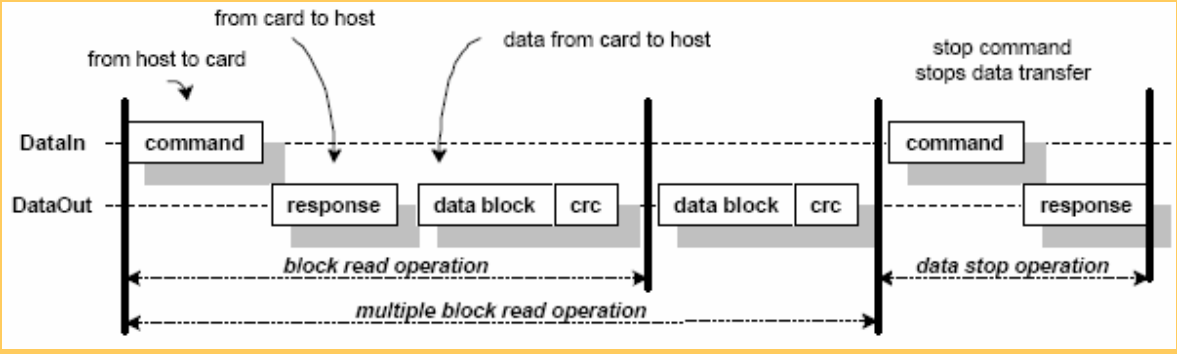
The response behavior in the SPI mode differs from the SD mode in the following three aspects:

- The selected card always responds to the command.
- Two new (8 & 16 bit) response structure is used
- When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than a time-out as in the SD mode.

In addition to the command response, each data block sent to the card during write operations will be responded with a special data response token.

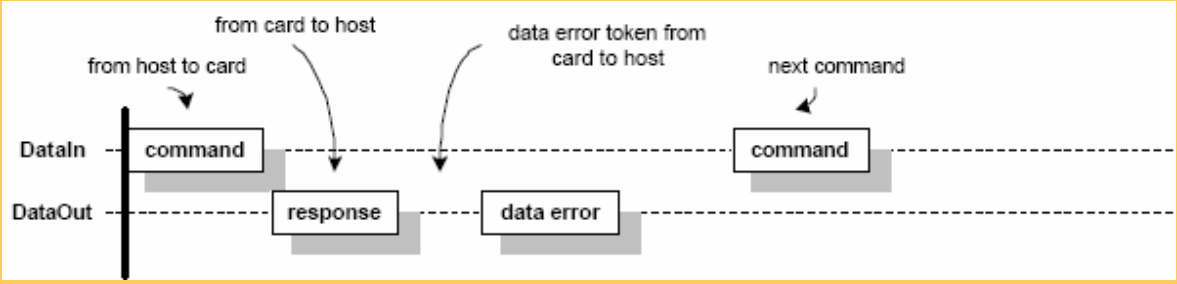
4.5 Data Read

Single and multiple blocks read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signals are used. Upon reception of a valid read command, the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command. A multiple block read operation is terminated, similar to the SD protocol, with the STOP_TRANSMISSION command.



Data read

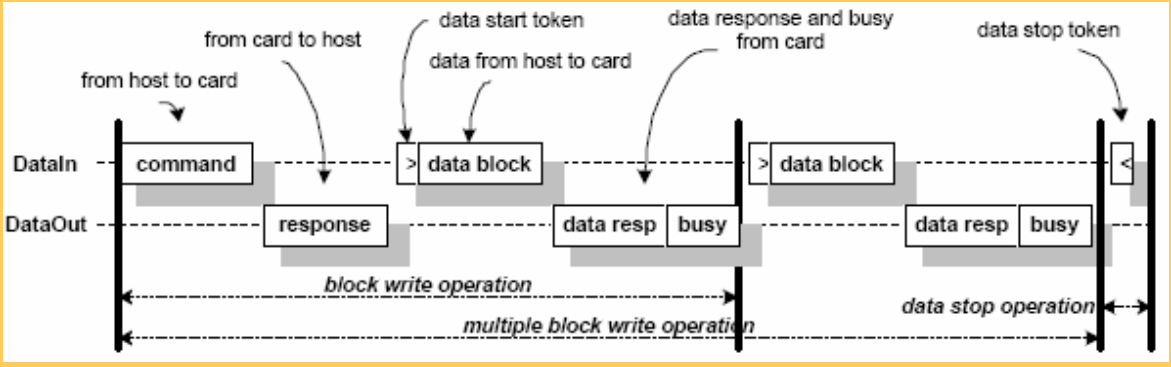
A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial $x^{16}+x^{12}+x^5+1$. In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure shows a data read operation, which terminated with an error token rather than a data block.



Read Operation - Data Error

4.6 Data Write

Single and multiple blocks write operations are supported in SPI mode. Upon reception of a valid write command, the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are identical to the read operation.

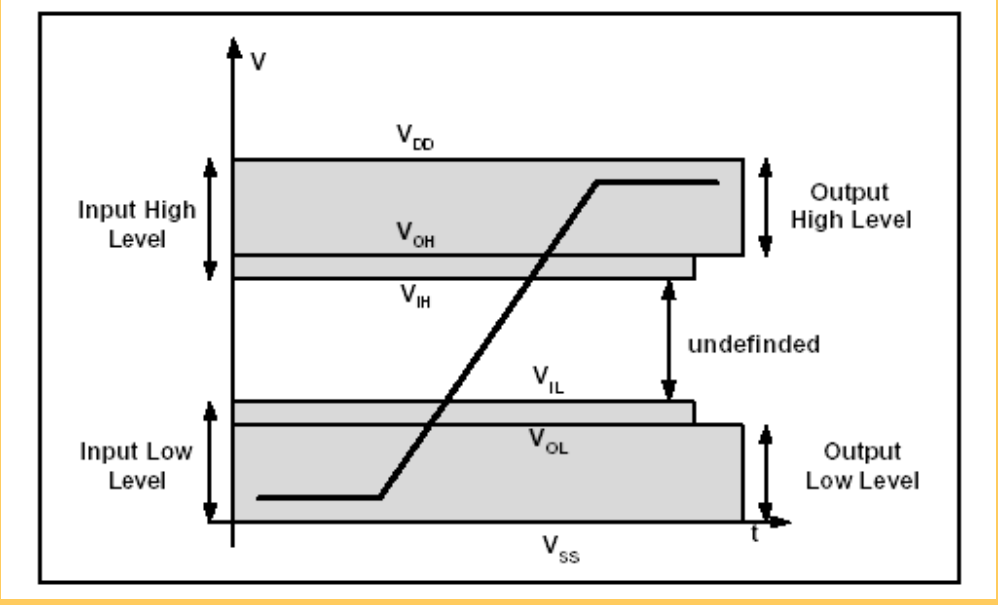


Write Operation

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

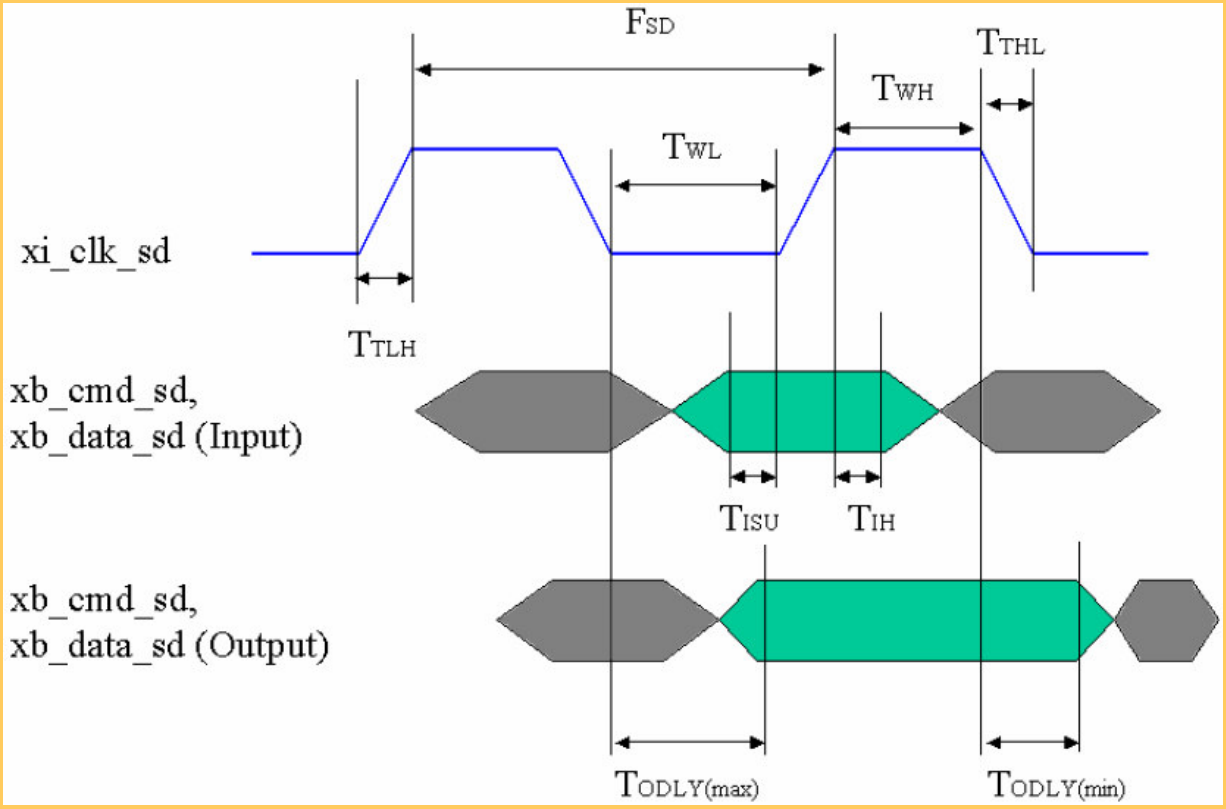
5 AC and DC CHARACTERISTICS

5.1 SD Signal Level



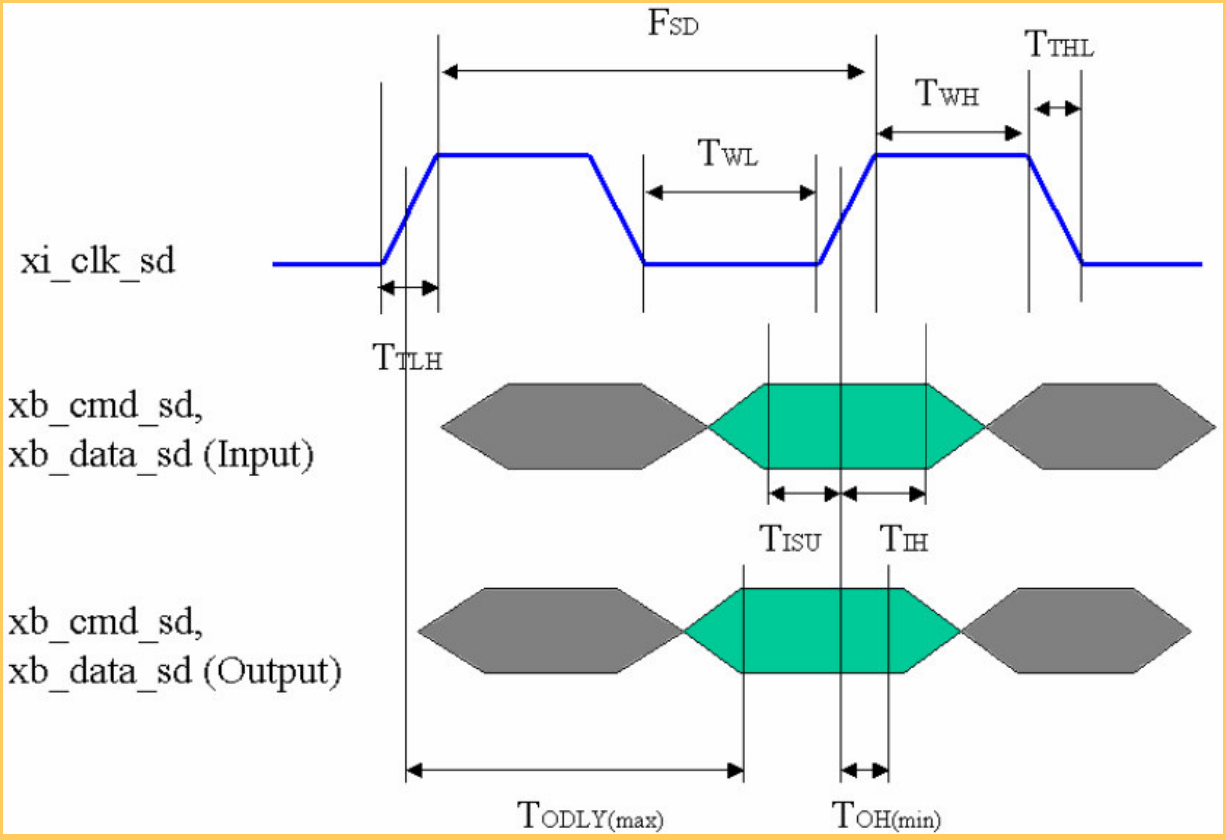
Parameter	Symbol	Min.	Max.	Unit	Conditions Output
Output High Voltage	V_{OH}	$0.75 \times V_{DD}$		V	IOH= -100μA @ VDD Min
Output Low Voltage	V_{OL}		$0.125 \times V_{DD}$	V	IOL=100μA @ VDD Min
Input High Voltage	V_{IH}	$0.625 \times V_{DD}$	$V_{DD} + 0.3$	V	
Input Low Voltage	V_{IL}	VSS - 0.3	$0.25 \times V_{DD}$	V	

5.2 Bus Timing (Default Mode)



Parameter	Symbol	Min.	Max.	Unit	Remark
SD clock frequency	f_{SD}	0	25	MHz	
Clock low time	t_{WL}	10		nS	
Clock high time	t_{WH}	10		nS	
Clock rise time	t_{TLH}		10	nS	
Clock fall time	t_{THL}		10	nS	
Input setup time	t_{ISU}	5		nS	
Input hold time	t_{IH}	5		nS	
Output delay time	t_{ODLY}	0	14	nS	

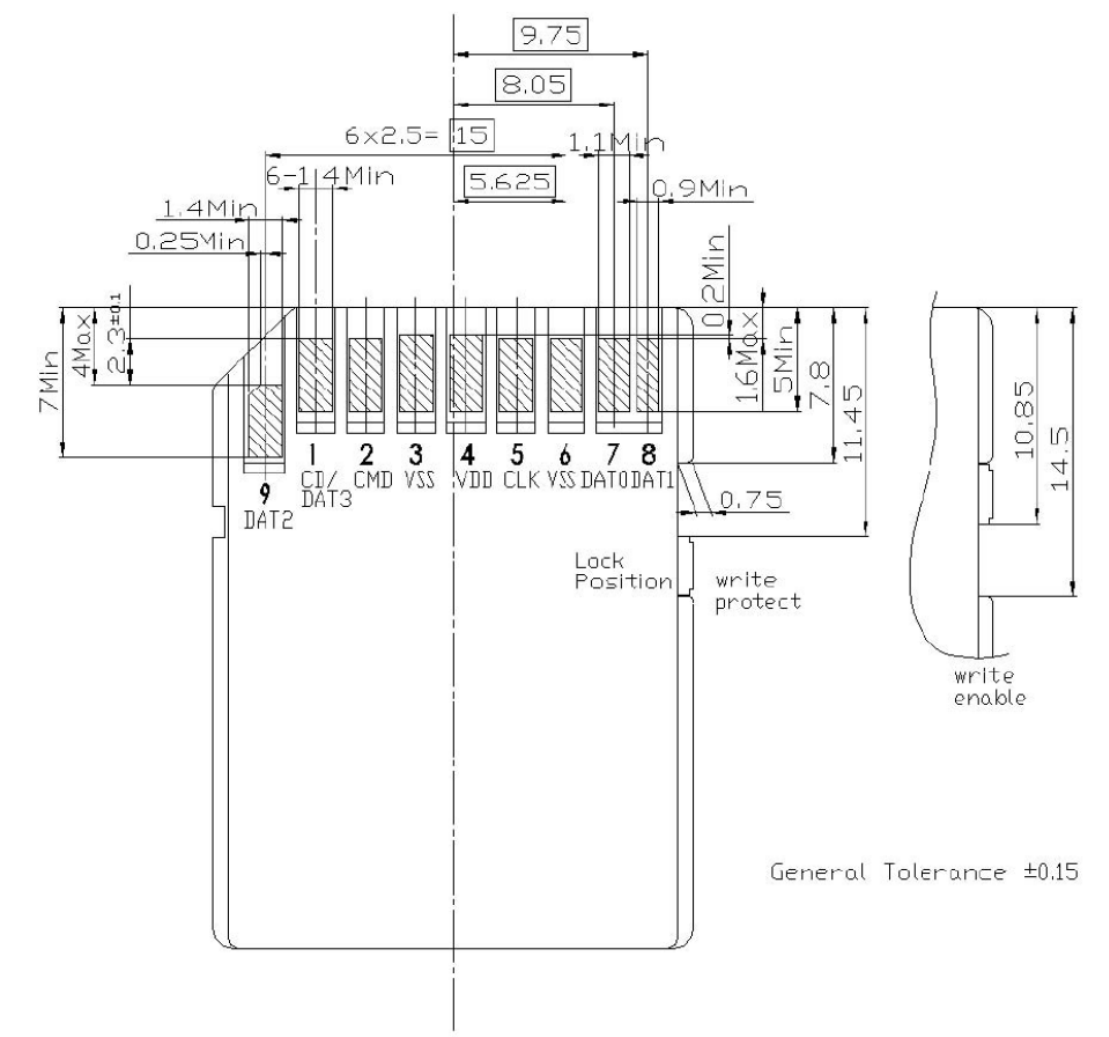
5.3 Bus Timing (High Speed Mode)

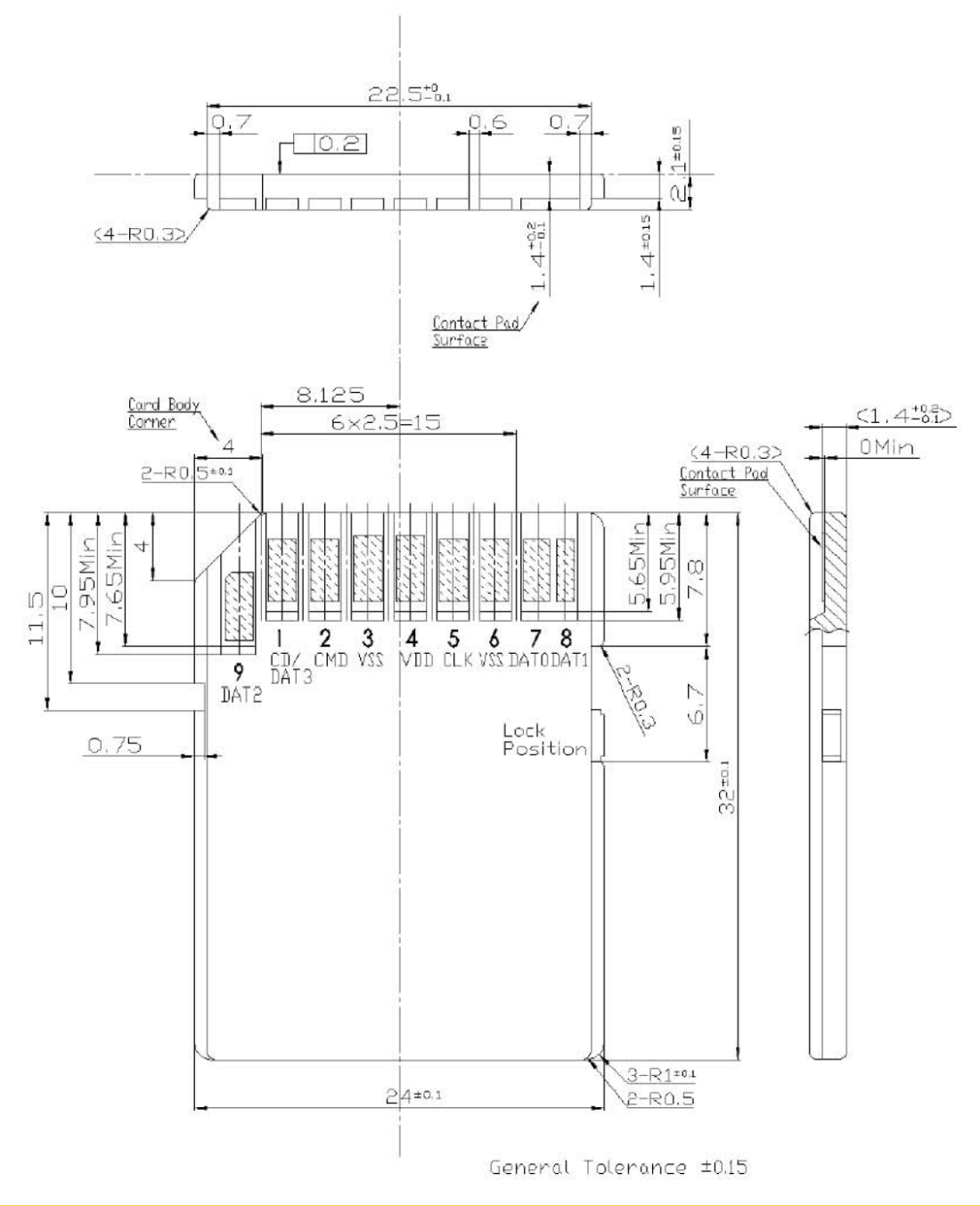


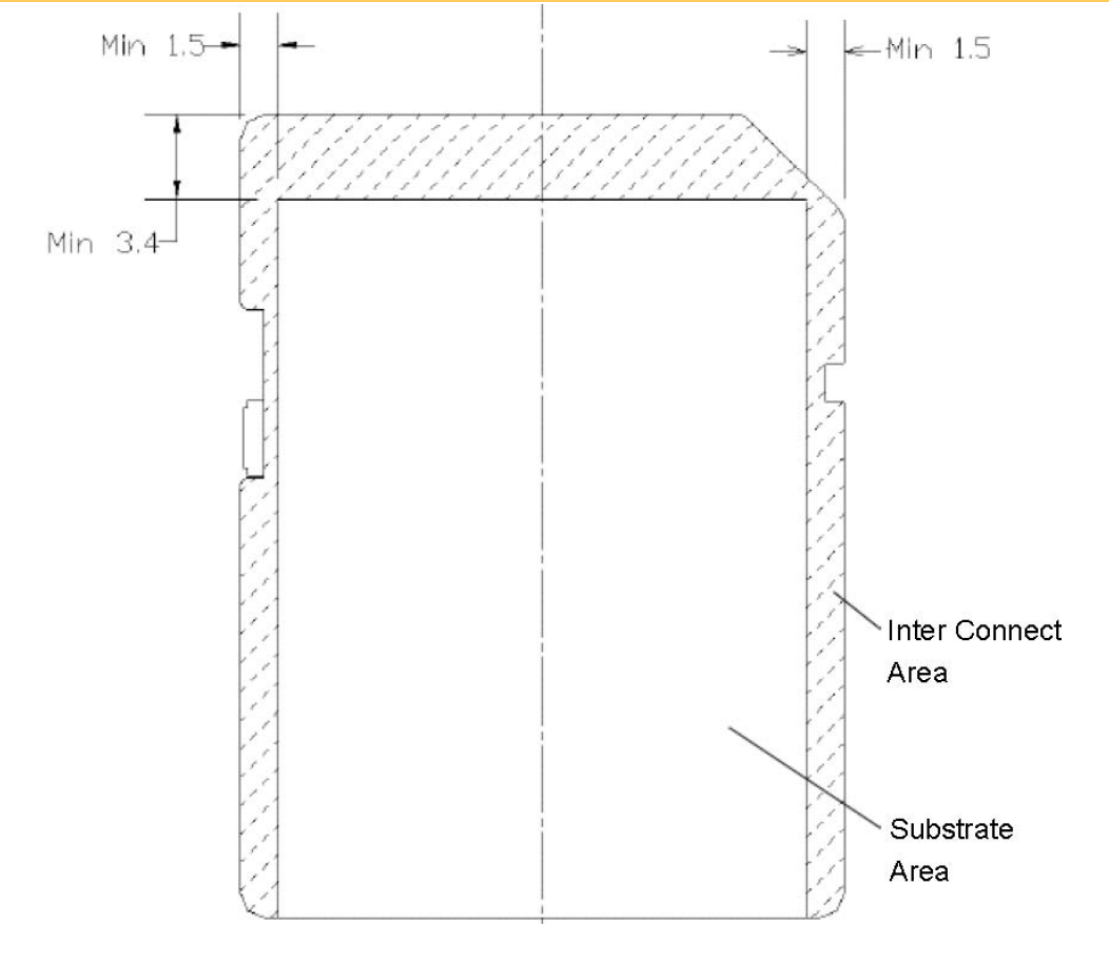
Parameter	Symbol	Min.	Max.	Unit	Remark
SD clock frequency	f_{SD}	0	50	MHz	
Clock low time	t_{WL}	7		nS	
Clock high time	t_{WH}	7		nS	
Clock rise time	t_{TLH}		3	nS	
Clock fall time	t_{THL}		3	nS	
Input setup time	t_{ISU}	6		nS	
Input hold time	t_{IH}	2		nS	
Output delay time	t_{ODLY}	0	14	nS	
Output hold time	t_{OH}	2.5		nS	

6 Physical Specifications

Parameter	Description
Weight	2.0g
Length	32+-0.10mm
Width	24+-0.10 mm
Thickness Excluding Lip	2.1mm+-0.15mm




22.5+0 -0.1
0.7
0.2
0.6
0.7
2.1±0.15
(4-R0.3)
1.4+0.2 -0.1
1.4±0.15
Contact Pad Surface
Card Body Corner
8.125
6×2.5=15
4
2-R0.5±0.1
(1.4+0.8 -0.1)
0Min
(4-R0.3)
Contact Pad Surface
11.5
10
7.95Min
7.65Min
4
5.65Min
5.95Min
7.8
1 2 3 4 5 6 7 8
CD/ DAT3 CMD VSS VDD CLK VSS DAT0 DAT1
9 DAT2
2-R0.3
6.7
0.75
Lock Position
32±0.1
3-R1±0.1
2-R0.5
24±0.1
General Tolerance ±0.15



Design and format	
Dimensions package	24mm x 32mm; (min. 23.9mm x 31.9mm; max.24.1mm x 2.1mm) other dimensions Figure 15 testing according to MIL STD 883, Meth 2016
thickness	Inter Connect Area: 2.1mm +/-0.15mm or 1.4mm+/-0.15mm for Thin SD Card. Substrate Are: Max 2.25mm or Max 1.55 for Thin SD Card
label or printable area	In 'Substrate Area' only
surface	plain (except contact area)
edges	smooth edges
inverse insertion	protection on left corner (top view)
position of ESC	contacts along middle of shorter edge

7 Ordering Information

7.1 Part Number

Capacity	Wide Temperature (－25℃~+85℃)
512MB	PCDSD512MBI
1GB	PCDSD1024MBI
2GB	PCDSD2048MBI
4GB	PCDSD4096MBI
8GB	PCDSD8192MBI